AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions, and listings, of claims in the application:

1   1. – 6. (Cancelled)

1   7.   (Currently Amended) A network interface for processing an incoming message
2   sent by a client device to a server, comprising:
3   a First-In-First-Out (FIFO) buffer adapted to receive the incoming message and to
4   assemble the incoming message from a serial to a parallel form;
5   a regular-expression pattern matching circuit connected to the FIFO buffer, the
6   regular-expression pattern matching circuit adapted to, concurrent with the assembly of the
7   incoming message from a serial to a parallel form, recognize a Hypertext Transfer Protocol
8   (HTTP) message header embedded in the incoming message, parse the recognized HTTP
9   message header into a parsed HTTP message header, provide the parsed HTTP message header
10   in a compact form to <u>a CPU and memory in</u> the server, and provide to <u>the CPU and memory in</u>
11   the server the incoming message that cannot be recognized by the regular-expression pattern
12   matching circuit, wherein:
13   the HTTP message header includes a HTTP cookie, and
14   the regular-expression pattern matching circuit is implemented by a technique
15   <u>selected from the group</u> consisting of hardware, software, and a combination thereof; and
16   a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a
17   response message to the client device based on a content of the recognized HTTP message
18   header.

1   8. – 12. (Cancelled)

2

1   13.   (Currently Amended) A server for providing services to a client device,

2   comprising:

3   a central processing unit (CPU);

4   a bus connected to the CPU;

5   a memory connected to the bus, the memory having a server application program stored

6   therein; and

7   a network interface for processing <u>an</u> incoming ~~messages~~ <u>message</u> sent by the client

8   device to the server, the network interface including:

9   a First-In-First-Out (FIFO) buffer adapted to receive the incoming ~~messages~~

10   <u>message</u> and to assemble the incoming ~~messages~~ <u>message</u> from a serial to a parallel form,

11   a regular-expression pattern matching circuit connected to the FIFO buffer, the

12   regular-expression pattern matching circuit adapted to, concurrent with the assembly of the

13   incoming ~~messages~~ <u>message</u> from a serial to a parallel form, recognize <u>a</u> Hypertext Transfer

14   Protocol (HTTP) message ~~headers~~ <u>header</u> embedded in the incoming ~~messages~~ <u>message</u>, parse

15   <u>the</u> recognized HTTP message ~~headers~~ <u>header</u> into <u>a</u> parsed HTTP message ~~headers~~ <u>header</u>,

16   provide the parsed HTTP message ~~headers~~ <u>header</u> in a compact form to the CPU and the

17   memory, and provide to the CPU and the memory <u>any</u> incoming ~~messages~~ <u>message</u> that cannot

18   be recognized by the regular-expression pattern matching circuit, wherein:

19   the HTTP message ~~headers include~~ <u>header includes an</u> HTTP ~~cookies~~ <u>cookie</u>, and

20   the regular-expression pattern matching circuit is implemented by a technique

21   <u>selected from the group</u> consisting of hardware, software, and a combination thereof, and

22   a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a

23   response message to the client device based on [[a]] content of the recognized HTTP message

24   ~~headers~~ <u>header</u>.

1   14. – 18. (Cancelled)

1   19.   (Currently Amended) A communications network comprising:

2   a client device; and

3   a server connected to the client device for providing services to the client device, the

4   server including:

5   a central processing unit (CPU),

6   a bus connected to the CPU,

7   a memory connected to the bus, the memory having a server application program

8   stored therein, and

9   a network interface for processing <u>an</u> incoming ~~messages~~ <u>message</u> by the client

10   device to the server, the network interface including:

11   a First-In-First-Out (FIFO) buffer adapted to receive the incoming

12   ~~messages~~ <u>message</u> and to assemble the incoming ~~messages~~ <u>message</u> from a serial to a parallel

13   form,

14   a regular-expression pattern matching circuit connected to the FIFO

15   buffer, the regular-expression pattern matching circuit adapted to, concurrent with the assembly

16   of the incoming ~~messages~~ <u>message</u> from a serial to a parallel form, recognize <u>a</u> Hypertext

17   Transfer Protocol (HTTP) message ~~headers~~ <u>header</u> embedded in the incoming ~~messages~~

18   <u>message</u>, parse the recognized HTTP message ~~headers~~ <u>header</u> into <u>a</u> parsed HTTP message

19   ~~headers~~ <u>header</u>, provide the parsed HTTP message ~~headers~~ <u>header</u> in a compact form to the CPU

20   and the memory, and provide to the CPU and the memory <u>any</u> incoming ~~messages~~ <u>message</u> that

21   cannot be recognized by the regular-expression pattern matching circuit, wherein:

22   the HTTP message ~~headers include~~ <u>header includes an</u> HTTP ~~cookies~~ <u>cookie</u>, and

23   the regular-expression pattern matching circuit is implemented by a technique

24   <u>selected from the group</u> consisting of hardware, software, and a combination thereof, and

25   a logic circuit connected to the FIFO buffer, the logic circuit adapted to provide a

26   response message to the client device based on a content of the recognized HTTP message

27   ~~headers~~ <u>header</u>.

1   20.   (Currently Amended) A method for processing an incoming message sent by a

2   client device to a server, comprising:

3   receiving the incoming message using a First-In-First-Out (FIFO) buffer;

4   assembling the incoming message from a serial to a parallel form using the FIFO buffer;

5   and

6   concurrent with the assembling of the incoming message from a serial to a parallel form:

7   recognizing a Hypertext Transfer Protocol (HTTP) message header embedded in

8   the incoming message received by the FIFO buffer using a regular-expression pattern matching

9   circuit,

10   parsing the recognized HTTP message header into a parsed HTTP message

11   header using the regular-expression pattern matching circuit, [[and]] <u>wherein the HTTP message</u>

12   <u>header includes a HTTP cookie</u>;

13   providing the parsed HTTP message header <u>in a compact form</u> to <u>a CPU and a</u>

14   <u>memory in</u> the server<u>;</u>

15   <u>providing a response message to the client device based on a content of the</u>

16   <u>recognized HTTP message header;</u>

17   <u>providing to the server any incoming message that cannot be recognized by the</u>

18   <u>regular-expression pattern matching circuit.</u>

1   21. – 25. (Cancelled)